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Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors

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The threshold voltage instabilities in nitride/oxide dual gate dielectric hydrogenated amorphous silicon (*a*-Si:H) thin-film transistors are investigated as a function of stress time, stress temperature, and stress bias. The obtained results are explained with a multiple trapping model rather than weak bond breaking model. In our model, the injected carriers from the *a*-Si:H channel first thermalize in a broad distribution of localized band-tail states located at the *a*-Si:H/*a*SiN_x:H interface and in the *a*-SiN_x:H transitional layer close to the interface, then move to deeper energies in amorphous silicon nitride at longer stress times, larger stress electric fields, or higher stress temperatures. The obtained bias-stress-temperature induced threshold voltage shifts are accurately modeled with a stretched-exponential stress time dependence where the stretched-exponent β cannot be related to the $\beta=T_{ST}/T_0$ but rather to $\beta\simeq T_{ST}/T_0^*-\beta_0$ for $T_{ST}\leqslant 80$ °C; for $T_{ST}\geqslant 80$ °C, the β is stress temperature independent. We have also found that β is stress gate bias independent.

The mechanism responsible for the threshold voltage shift in nitride gate insulator transistors under time, temperature, and positive bias stress conditions is attributed in the literature to two possible degradation mechanisms: charge trapping in the gate insulator[1–4] and the creation of dangling bond defects in the *a*-Si:H channel[5–7] near the *a*-SiN_x:H/*a*-Si:H interface. Because of this conflict, there is a need to clarify some of the important questions concerning both these mechanisms before any final conclusions can be reached regarding the *a*-Si:H TFT's instability. The present letter is an attempt to provide some additional insight concerning the TFT's instability.

The transistors employed in this study are the inverted staggered type,[8] with $W/L=100/16$. The bottom Mo gate electrode is covered with a PECVD (plasma enhanced chemical vapor deposition) dual insulator of 300 nm *a*-SiO_x:H and 50 nm *a*-SiN_x:H (N-rich nitride) followed *in situ* by a 60 nm *a*-Si:H layer and a final passivating silicon nitride layer. All the layers have been deposited at 350 °C. The n^+-*a*-Si:H followed by Mo formed the source and drain contacts.

Each threshold voltage shift, ΔV_t, induced by BTS (bias-temperature-stress) was measured first *in situ* during the positive gate bias stress with drain voltage $V_d=0.5$ V by monitoring the drain current[9] and converting it to ΔV_t. The ΔV_t obtained by this method was then reconfirmed through a linear least square line fit method to the TFT transfer characteristics in the linear operating regime; ΔV_t is obtained by extrapolating to the gate voltage axis. The advantage of the first method is no interruption of the gate bias stress sequence, and hence, no charge relaxation from interfacial trapping levels (fast trap time constants) in the time between ending the bias stress condition and the start of threshold voltage measurements. Note that the detrapping (charge backtunneling) observed during the second method[8] is not compatible with the bond breaking model but is compatible with the charge trapping model under controlled conditions, gate insulator/interface trapping/detrapping is reversible. A disadvantage of only monitoring the *in situ* drain current during bias stress conditions is that the *a*-Si:H surface potential at the *a*-SiN_x:H gate interface is changing as a function of charge trapping, and also, one must assume a parallel transfer characteristic since only one drain current versus gate voltage value is recorded for a given stress time. Both extraction methods give approximately the same ΔV_t for a given BTS condition. A new device was selected upon each completion of the BTS. Finally, we should point out that all TFTs have been annealed at 180 °C before BTS and bias-stressed TFTs annealed at the same temperature can completely recover the virgin (unstressed) transfer characteristics. Identical TFT transfer characteristics have been obtained for virgin and for stressed/annealed TFTs.

Figure 1 shows the evolution of typical experimental transfer characteristics after positive gate bias stress, V_{ST}, of 30 V for different stress times, t_{ST}, which are indicated on the figure. These transfer characteristics show a sharp *ON/OFF* transition with about six and eight orders of magnitude on the *ON/OFF* current ratio for V_d of 0.1 and 10 V, respectively. The inverse subthreshold slope and mobility are on the order of 850 mV/dec and 0.8 cm^2/V s, respectively. Note, under positive bias stress there is a parallel shift (negligable change in subthreshold slope, $\partial \log I_s/\partial V_g$, or transconductance, $\partial I_s/\partial V_g$) in the transfer characteristics to higher gate voltages with increasing stressing time. A similar parallel shift towards more negative gate voltages under negative bias stress is also observed.[1,8] This positive ΔV_t shift for positive stress gate biases and negative ΔV_t shift for negative stress gate biases result is indicative of gate insulator charge trapping. For larger stress bias fields across the gate insulator ($\gtrsim 1.7$ MV/cm at $\simeq 300$ °C), slight subthreshold slope and transconductance degradation with increasing stress time becomes noticeable, possibly attributed to a secondary instability such as field induced interface state creation. This point will be discussed in a separate publication. Even at

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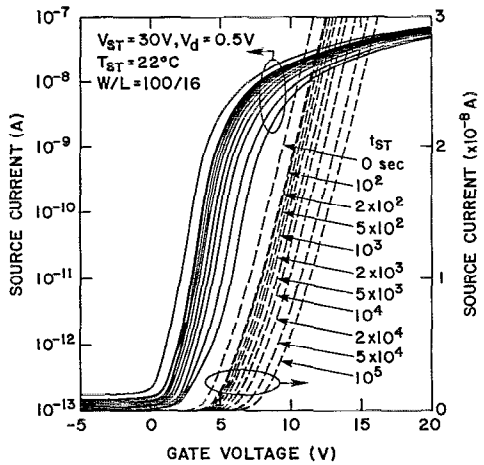

FIG. 1. Effect of 30 V gate bias stress on the subthreshold (solid line) and linear region (dashed lines) transfer characteristics of an inverted-staggered a-Si:H thin-film transistor incorporating a 50 nm N-rich nitride/200 nm oxide gate dielectric and a 60-nm-thick a-Si:H layer with transistor dimensions of $W/L=100/16$. In all cases, the gate dielectric, the intrinsic a-Si:H channel and the P-doped S/D contact layers have been deposited at 250 °C. During bias stress and measurement $V_d=0.5$ and 0.1 V, respectively. Note that the increasing stress times from 0 (unstressed) to 10^5 s shown in the figure produce a parallel shift of the transfer characteristics with an increase in the threshold voltage.

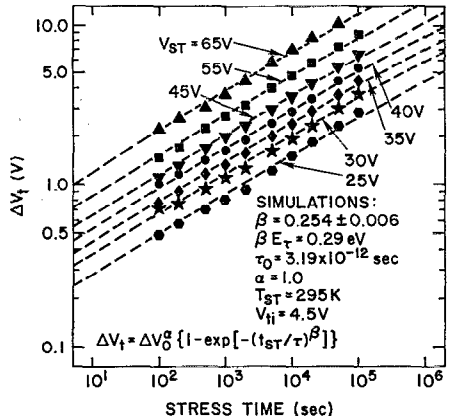

FIG. 2. Threshold voltage shift, ΔV_t, vs stress time for gate bias stress voltages ranging from 25 to 65 V and $T_{ST}=22$ °C. The symbols represent the data and the dashed lines the fits to Eq. (1) with the parameter values used listed in this figure.

the higher gate insulator fields approaching 2 MV/cm, the TFT threshold voltage shift is still primarily due to gate insulator charge trapping. Since the primary TFT instability is associated with charge trapping at the a-SiN_x/a-Si:H interface and in the gate insulator near the interface, the trapped charge must be correctly accounted for in simulations by employing a stress time dependent flatband voltage value; if one assumes the flatband voltage shift ΔV_{fb} equals zero during BTS, it is obvious that the ΔV_t shift must be associated with state creation in the a-Si:H layer.

In contrast to the previous publications[5–7] and based on our previously published[1,8] and present letter's experimental data, we interpret our threshold voltage shift data to be the result of charge injection from the a-Si:H channel into traps located at the a-Si:H/a-SiN_x:H interface and in the gate insulator near the interface. The ΔV_t shift in the transfer characteristics of all transistors in this investigation are well described by the stretched-exponential equation[1]

$$|\Delta V_t| = |\Delta V_0|\left\{1-\exp\left[-\left(\frac{t_{ST}}{\tau}\right)^{\beta}\right]\right\}, \qquad (1)$$

where ΔV_0 is approximately the effective voltage drop across the insulator, $\tau=\tau_0\exp(E_\tau/kT)$ represents the characteristic trapping time of carriers where the thermal activation energy is given by $E_a=E_\tau\beta$, with β being the stretched-exponential exponent. In our model, $E_\tau=E_a/\beta$ in Eq. (1) is the average effective energy barrier that carriers in the a-Si:H channel need to overcome before they can enter the insulator, with τ_0 being the thermal prefactor for emission over the barrier. For shorter stress times, smaller stress electrical fields, or lower stress temperatures, carriers hop or inject directly into lower energy states located at the a-Si:H/a-SiN_x:H interface and in the a-SiN_x:H transitional layer close to the interface; at longer stress times, larger stress electrical fields, or higher stress temperatures, a larger fraction of states in the insulator near the interface will become filled, giving rise to an increasing probability of emission from these states. It is plausible that the amorphous structure of the gate insulator will lend itself to an appreciable number of band-tail states which will act as transport states for the emitted lower energy trapped state charge. This distribution of multiple traps yields a time dependent power law.[11,12] Therefore, during the trapping there are many trapping events and the motion between traps is nondispersive diffusive motion with a superimposed drift velocity. This type of carrier transport and trapping could be well characterized by a stretched-exponential function given by Eq. (1).

The variation of the threshold voltage shift with the stress time for stress gate biases ranging from 25 to 65 V ($\simeq$0.6 to $\simeq$2 MV/cm) is shown in Fig. 2 in the $\log(\Delta V_t)$ versus $\log(t_{ST})$ plot. Simulations using Eq. (1) are overlayed on the measured data in Fig. 2, with $\beta=0.254\pm0.006$. ΔV_0 is set equal to the approximate effective potential drop at the interface, or $\Delta V_0\simeq(V_{ST}-V_{ti})$, with initial threshold voltage $V_{ti}\simeq4.5V$, $\tau_0\simeq3.19$ ps, and $E_\tau\simeq1.17$ eV. From this figure, it is clear that a power-law stress time dependence can describe each characteristic. Furthermore, an equal spacing in log stress time for decreasing gate bias stress indicates that β and τ is stress bias independent while ΔV_0 has a dependence on gate bias stress: In our simulations, we have set ΔV_0 in Eq. (1) directly equal to V_g-V_{ti}, with no power dependence, i.e., $\alpha\simeq1.0$. These results are in contradiction with previously published data[13,14] indicating that $\Delta V_t\propto(V_{ST})^\alpha(\log t_{ST})^\beta\times\exp(-\Delta E/kT)$ with $\alpha\neq1$, and $\beta\neq1$. In a later publication, Kaneko, Sassano, and Tsukada[15] has indicated that a better expression for the time dependence might have the form t^β, with the new formula for insulator trapped charge, Q, given by $Q\propto(E_{ST})^\alpha t_{ST}^\beta\exp(-\Delta E/kT)$ where E_{ST} is the gate insulator stress electric field.

The variation of ΔV_T with the stress temperature

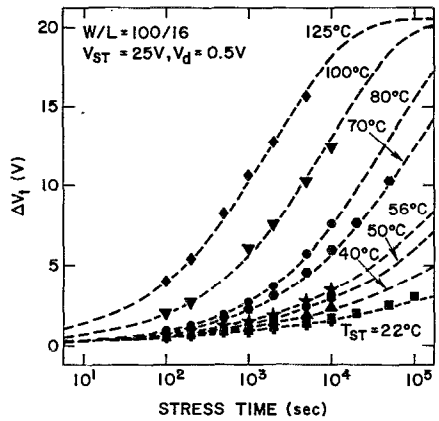

FIG. 3. Threshold voltage shift, ΔV_t, vs stress time for different stress temperatures ranging from 22 to 125 °C and for a positive gate bias of 25 V. The symbols represent the data and the dashed lines the fit to Eq. (1) with the parameter values used listed in Fig. 2.

(T_{ST}) for different stress times is shown in Fig. 3. A constant gate bias stress of 25 V was applied from room temperature upwards to 125 °C. At higher stress temperatures and stress times $\geqslant 10^4$ s, the TFTs exhibit noticeable leakage currents and have therefore not been included. The simulations shown with the dashed lines indicate that the experimental data given in this figure are consistent with Eq. (1). The evolution of log τ, obtained from the fitting of experimental data with Eq. (1), as a function of T^{-1} is shown in Fig. 4. From the slope of this curve, the activation energy $E_\tau = E_a/\beta$ on the order of 1.17 eV can be obtained and $(\tau_0)^{-1} \simeq 3.13 \times 10^{11}$ s^{-1}; for $V_{ST} = -30$ V, $E_\tau \approx 0.97$ eV and $\beta \approx 0.22$ eV have also been obtained. These

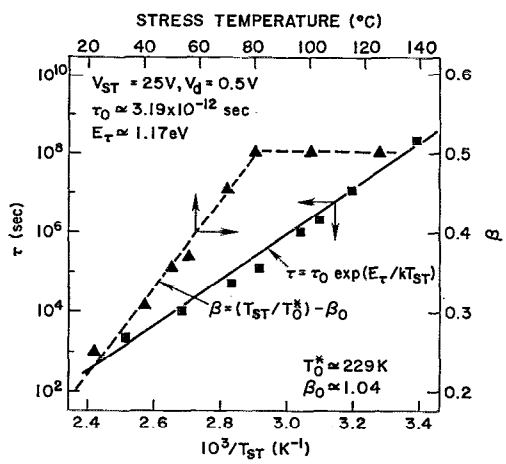

FIG. 4. The variation of the extracted fitting parameters of τ and β as a function of stress temperature. The squares and triangles represent extracted values from the data of Fig. 2, and the lines represent the bests fits to these data.

results are in good agreement with others.[1,5,6,11] According to the Si-Si weak bond breaking model proposed by Jackson, Marshall, and Moyer,[6] to explain the TFT bias instability, the hypothesis is that dispersive hydrogen diffusion causes the stretched-exponential behavior of ΔV_t with stress time. This model also predicts $\beta = T_{ST}/T_0$, (necessitating $\beta_0 = 0$) where kT_0 is the characteristic width of the distribution of hydrogen hopping energies and where T_0 is roughly 600 K for hydrogen diffusion and 700 K for the near-interface-state generation.[6] Our results in Fig. 4 show a different relationship for β. When $T_{ST} \leqslant 80$ °C, $\beta \simeq (T_{ST}/T_0^*) - \beta_0$, where $T_0^* \simeq 229$ K and $\beta_0 \simeq 1.04$. For $T_{ST} \geqslant 80$ °C, β becomes stress temperature independent with a β value of about 0.5. A careful examination of the β vs T_{ST} plot of Ref. 6 reveals that a linear least square fit of the data represented by the diamonds may also support the conclusion that $\beta_0 \neq 0$ and agrees more closely with our value. A similar observation was also made by Powell *et al.*,[7] although it lacked explanation. Therefore, a nonzero β_0 casts doubt on the conclusion drawn by different groups that threshold voltage instabilities in *a*-Si:H TFTs depend on hydrogen-diffusion-controlled creation in the *a*-Si:H film near the *a*-SiN_x:H/*a*-Si:H interface; ΔV_t in this model implies no dependency on the gate dielectric. We have observed a different threshold voltage shift when nitride is replaced by oxide gate dielectric. This observation supports the charge trapping model discussed in this letter.

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